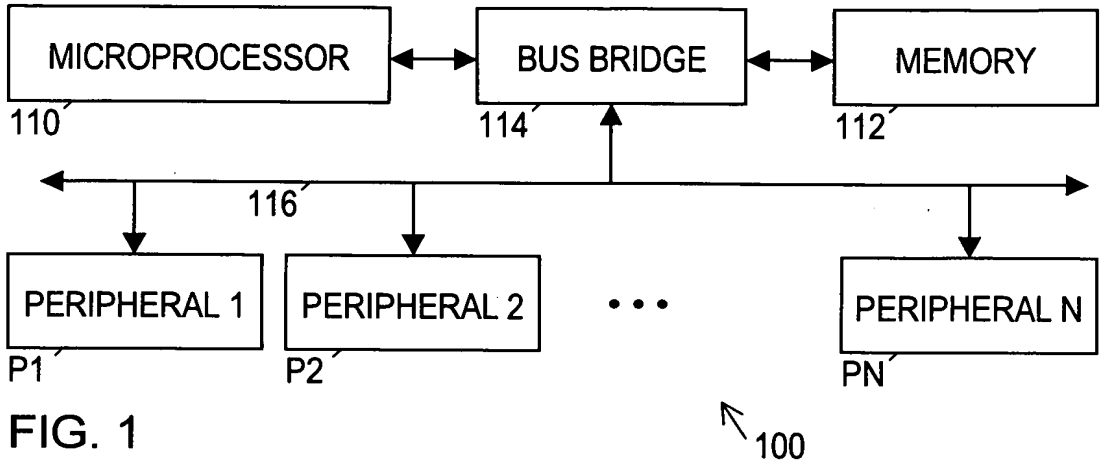
MICROPROCESSOR
110
BUS BRIDGE
114
MEMORY
112
116
PERIPHERAL 1
P1
PERIPHERAL 2
P2
PERIPHERAL N
PN
100

FIG. 1

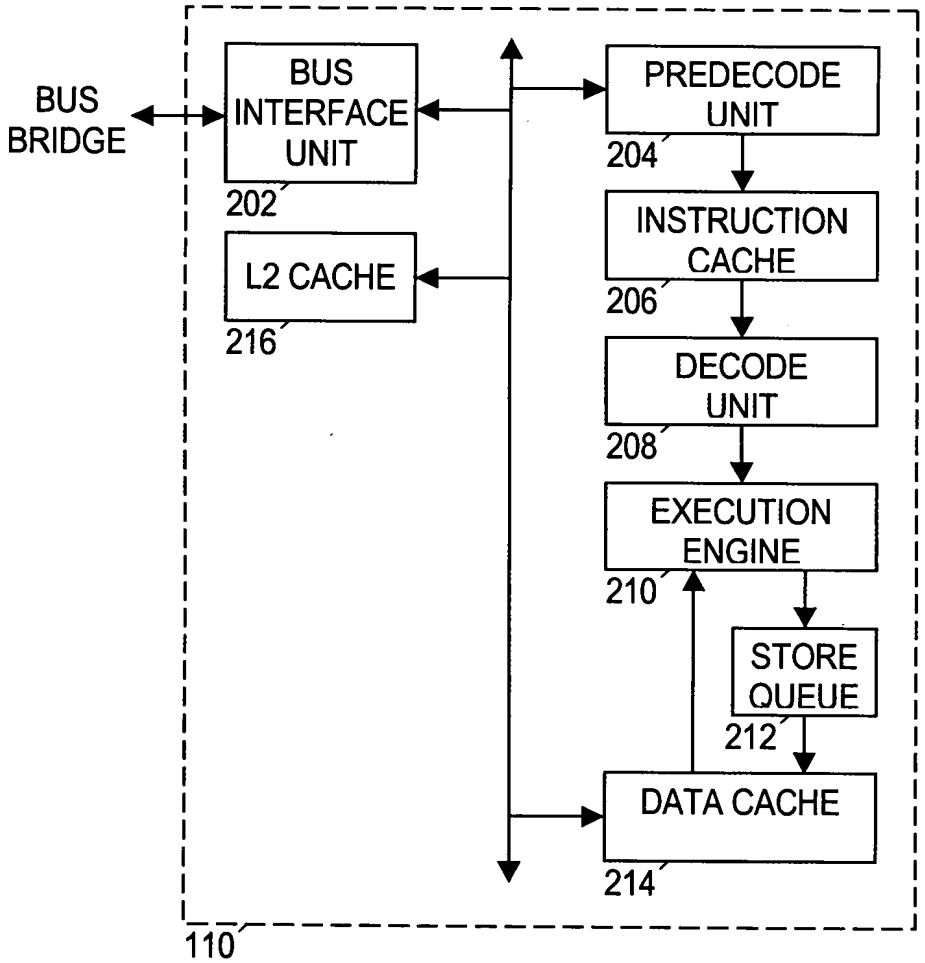
BUS BRIDGE
BUS INTERFACE UNIT
202
L2 CACHE
216
PREDECODE UNIT
204
INSTRUCTION CACHE
206
DECODE UNIT
208
EXECUTION ENGINE
210
STORE QUEUE
212
DATA CACHE
214
110

FIG. 2

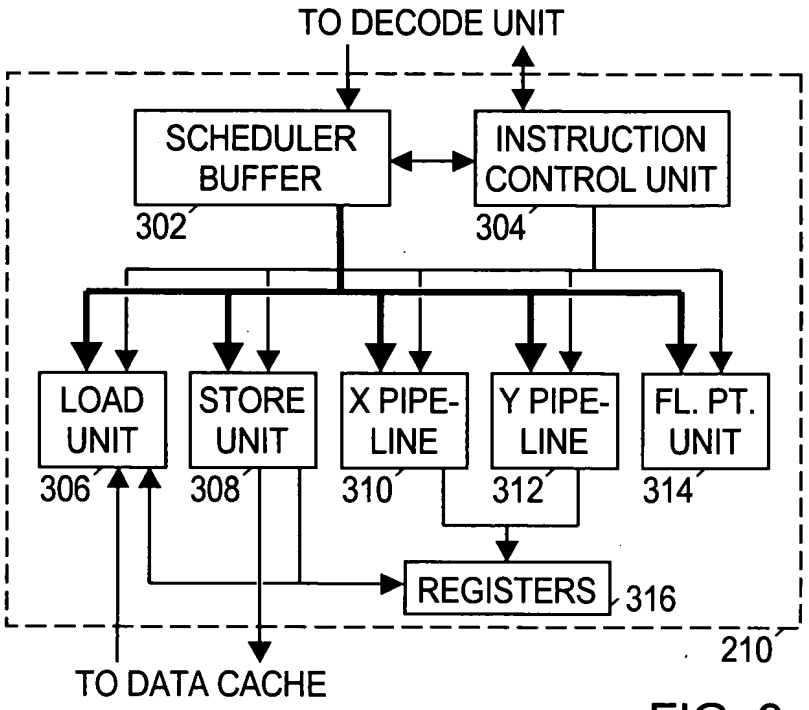

FIG. 3

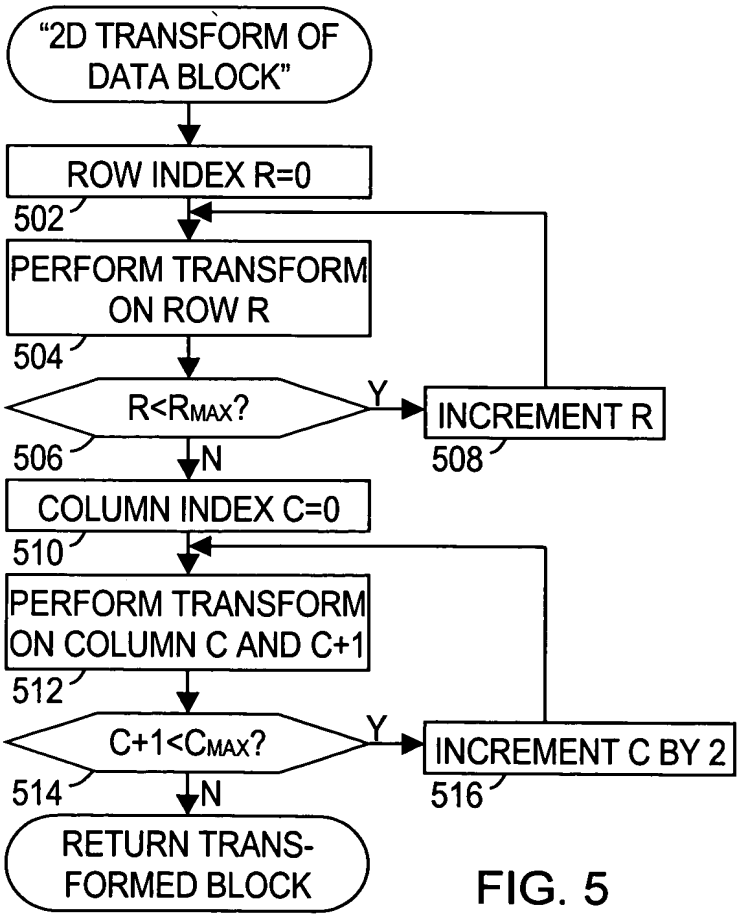

FIG. 5

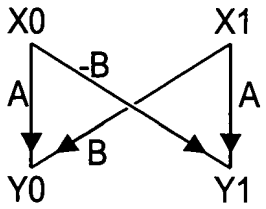

FIG. 6

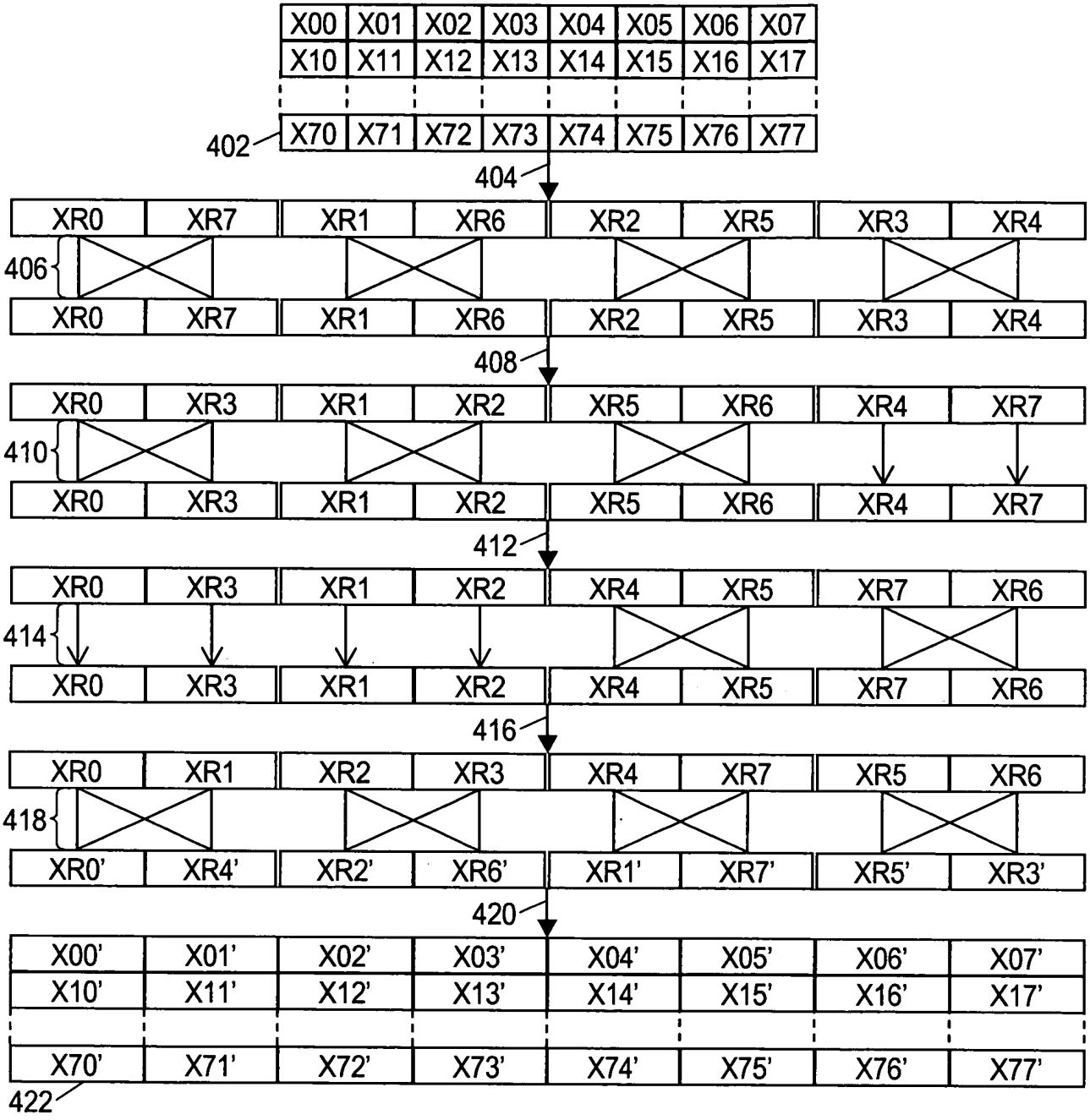
X00 X01 X02 X03 X04 X05 X06 X07
X10 X11 X12 X13 X14 X15 X16 X17
X70 X71 X72 X73 X74 X75 X76 X77
402
404
XR0 XR7 XR1 XR6 XR2 XR5 XR3 XR4
406
XR0 XR7 XR1 XR6 XR2 XR5 XR3 XR4
408
XR0 XR3 XR1 XR2 XR5 XR6 XR4 XR7
410
XR0 XR3 XR1 XR2 XR5 XR6 XR4 XR7
412
XR0 XR3 XR1 XR2 XR4 XR5 XR7 XR6
414
XR0 XR3 XR1 XR2 XR4 XR5 XR7 XR6
416
XR0 XR1 XR2 XR3 XR4 XR7 XR5 XR6
418
XR0' XR4' XR2' XR6' XR1' XR7' XR5' XR3'
420
X00' X01' X02' X03' X04' X05' X06' X07'
X10' X11' X12' X13' X14' X15' X16' X17'
X70' X71' X72' X73' X74' X75' X76' X77'
422

FIG. 4A

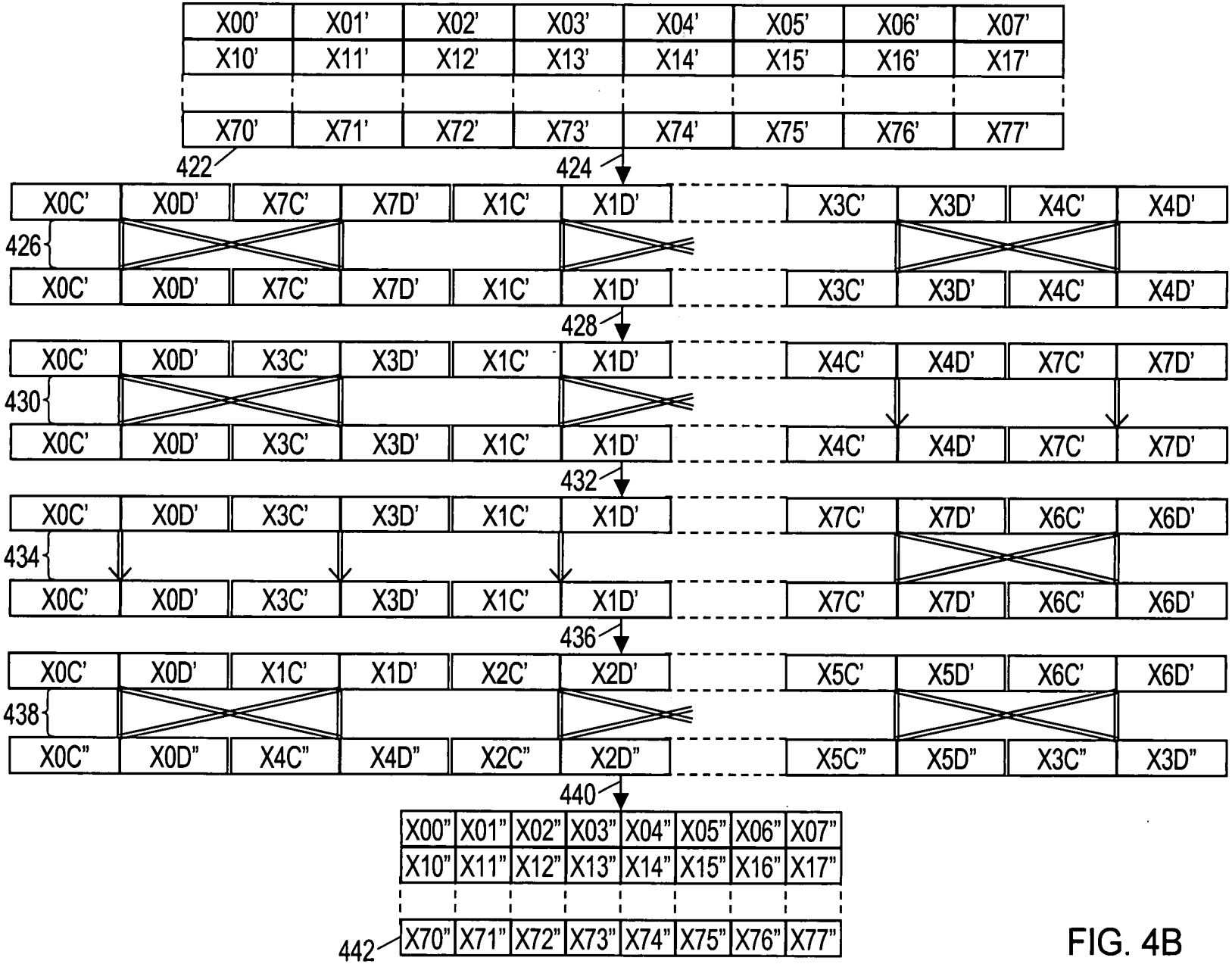
X00' X01' X02' X03' X04' X05' X06' X07'
X10' X11' X12' X13' X14' X15' X16' X17'
X70' X71' X72' X73' X74' X75' X76' X77'
422
424
X0C' X0D' X7C' X7D' X1C' X1D' X3C' X3D' X4C' X4D'
426
X0C' X0D' X7C' X7D' X1C' X1D' X3C' X3D' X4C' X4D'
428
X0C' X0D' X3C' X3D' X1C' X1D' X4C' X4D' X7C' X7D'
430
X0C' X0D' X3C' X3D' X1C' X1D' X4C' X4D' X7C' X7D'
432
X0C' X0D' X3C' X3D' X1C' X1D' X7C' X7D' X6C' X6D'
434
X0C' X0D' X3C' X3D' X1C' X1D' X7C' X7D' X6C' X6D'
436
X0C' X0D' X1C' X1D' X2C' X2D' X5C' X5D' X6C' X6D'
438
X0C" X0D" X4C" X4D" X2C" X2D" X5C" X5D" X3C" X3D"
440
X00" X01" X02" X03" X04" X05" X06" X07"
X10" X11" X12" X13" X14" X15" X16" X17"
X70" X71" X72" X73" X74" X75" X76" X77"
442

FIG. 4B